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Code No: A6508

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, October/November-2011
LOW POWER VLSI DESIGN
(WIRELESS AND MOBILE COMMUNICATIONS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1. (a) What are the limitations of Low Power Design?
   (b) Explain how SOI technology offer Low power operations? [6+6]

2. (a) Draw the Cross-sectional diagram of Standard buried collector BiCMOS structure and explain its process.
   (b) Explain the LOCOS technology for isolation of silicon IC fabrication. [6+6]

3. (a) Explain the process flow for Polysilicon emitter formation in BiCMOS structure.
   (b) How a double-polysilicon self-aligned bipolar device improve the performance of BiCMOS devices? [6+6]

4. What are the different advanced MOSFET models? Explain them with suitable diagrams. [6+6]

5. (a) How the short-channel effects on the threshold voltage model of submicron MOS devices?
   (b) How the Source/drain and source/body voltages are modified in temperature dependent Hybrid-model device model. [6+6]

6. (a) Draw the circuit diagram of BiCMOS buffer and explain its working.
   (b) Draw the basic two-input NAND gate in conventional CMOS technology and explain its operation with truth table. [6+6]

7. (a) Draw the ESD-free BiCMOS inverter circuit and explain its working.
   (b) Compare the performance characteristics of ESD-free BiCMOS circuits with Conventional MOS Circuits. [6+6]

8. (a) What are the uses of latches and flip-flops?
   (b) Explain the performance measures for latches and flop-flops. [6+6]

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